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Awarded Runner-up REV2021 Best Full Paper Award


Using online learning, remote FPGA prototyping and course builder platform

Presentation Video

https://tinyurl.com/RISCVOntlineTutorLinks
Presentation Overview

• RISC-V introduction
• RISC-V Online Tutor course strategy and demo
• vicilogic Online learning, remote FPGA prototyping, course builder
• RISC-V Online Tutor lesson structure and application program demos
• RISC-V Online Tutor user experience and feedback, FPGA usage stats
• Future work (inviting Community participation/collaboration)
About RISC-V

- Free, open Instruction Set Architecture (ISA) (Berkeley 2010)
- Growing community (RISC-V International, industry, university)
- Enabling new era of processor innovation
  - through open standard collaboration
  - Freedom in developing extensible software and hardware
- Custom ICs based on RISC-V will enable cost-effective IoT product differentiation
  - Building custom chips becoming practical, due to evolution of electronic design tools, and lower market entry to semiconductor manufacturing industry
  - Sustainable choice for building custom chips, thanks to adoption/promotion by major technology companies, industrial organisations, governments

(Gartner Report, June 20)
Training: Call For Participation

• Bare Metal & Real-time OS on RISC-V
• Compliance & Verification
• Debug & Trace
• Formal Specification
• Physical Memory Protection
• The RISC-V Memory Model
• RISC-V Toolchain & Kernel Development

riscv.org
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• **RISC-V Online Tutor course strategy and demo**

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Visualising RV32I RISC-V Architecture

Single cycle datapath diagram

Online Tutor datapath diagram

Online Tutor: Audience/Strategy

• Target audience
  • Professors/Students, Embedded Systems/IP Developers, Programmers
    ... interested in RISC-V Fundamentals; what’s Inside a RV32I RISC-V processor?

• Integrated training and practice (15 hours online, excluding labs)
• From RISC-V digital logic hardware to C programming
• Lesson strategies
  • Online, self-paced
  • Integrated with remote RISC-V hardware
  • Interactive, learn-by-doing experience, visually-rich
  • Guided-learning, sandboxes, knowledge checks
Course Structure

From RISC-V digital logic hardware to C programming
A. Front: introduction, resources, references
B. Tools tutorials
   • Assembly language Venus [7] online simulator
   • Remote RISC-V hardware: program instruction upload, execute, hardware debug
C. RV32I assembly instruction-by-instruction -- processor hardware support
D. RV32I RISC-V hardware design-to-prototype (HDL-based), with memory-mapped peripherals, using industry-standard tools / hardware description language (HDL)
E. Assembly program applications (including games)
F. Advanced Topics: pipelining/hazards, C-to-assembly
Lesson/Framework Demo

- Register-immediate instruction
- Guided lesson
- Browser (view on left side) links to remote RISC-V hardware
- Overlays signal widgets on view
- **highlight active datapaths
- Remote FPGA tower
- Transparent FPGA allocation, FPGA configuration, browser-FPGA interaction

![Diagram showing ALU, RB Register Bank x0-x15, and x10/x11 LED display]
### Detailed Course Structure

<table>
<thead>
<tr>
<th>Section/Topics</th>
<th>Duration (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A. Intro, resources, references, application demos</strong></td>
<td></td>
</tr>
<tr>
<td>1. Introduction: RISC-V Processor Architecture &amp; Applications</td>
<td>90</td>
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<tr>
<td>2. Learning Outcomes RV32I RISC-V instruction generator and viewer</td>
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<tr>
<td>2. RV32I RISC-V instruction generator and viewer</td>
<td></td>
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<tr>
<td>3. RISC-V references</td>
<td></td>
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<tr>
<td>4. Tour of vicilogic online learning and prototyping platform</td>
<td></td>
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<tr>
<td>5. Game application demos (executing on remote RISC-V)</td>
<td></td>
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<tr>
<td><strong>B. Program execution tools tutorials (simulation/remote hardware)</strong></td>
<td></td>
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<tr>
<td>5. Assembly programming, simulate, hardware execution and debug</td>
<td>120</td>
</tr>
<tr>
<td><strong>C. RV32I assembly instructions and processor architecture support</strong></td>
<td></td>
</tr>
<tr>
<td>6. addi register-immediate</td>
<td>120</td>
</tr>
<tr>
<td>7. add/sub register-register</td>
<td>40</td>
</tr>
<tr>
<td>8. Register-immediate addi, xori, ori, andi, sli, sltu</td>
<td>60</td>
</tr>
<tr>
<td>9. Register-register add, sub, xor, or, and, sli, sltu</td>
<td>20</td>
</tr>
<tr>
<td>10. Constant-shift slli, srli, srai, register-shift sll, srl, sra</td>
<td>35</td>
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<tr>
<td>11. lui load upper immediate</td>
<td>15</td>
</tr>
<tr>
<td>12. beq, bne, blt, bge, bitu, bgeu branch</td>
<td></td>
</tr>
<tr>
<td>Program: delay loop</td>
<td>50</td>
</tr>
<tr>
<td>13. Program: shift x10 register left each sec lui, add, addi, slli, bne</td>
<td>25</td>
</tr>
<tr>
<td>14. Store/load to/from memory sw, sh, sb, lw, lh, lb, lh, lhu, lbu</td>
<td>60</td>
</tr>
<tr>
<td>15. auipc add upper immediate to PC</td>
<td>20</td>
</tr>
<tr>
<td>16. jal/jalr jump and link</td>
<td>25</td>
</tr>
<tr>
<td>**D. RV32I Processor hardware design (HDL capture-to-prototype),</td>
<td></td>
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<tr>
<td>memory-mapped peripherals</td>
<td></td>
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<tr>
<td>17. IF PCCU/IM, ID DEC/RB, EX EX/ALU, MEM memory, WB writeback</td>
<td>30</td>
</tr>
<tr>
<td>18. RV32I Hardware Description Language model capture, simulation, logic</td>
<td></td>
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<tr>
<td>synthesis, prototype (remote FPGA)</td>
<td></td>
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<tr>
<td>19. Memory-mapped peripheral components applications</td>
<td>45</td>
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<tr>
<td><strong>E. Assembly program applications (game app development)</strong></td>
<td></td>
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<tr>
<td>20. Functions and stack handling</td>
<td>40</td>
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<tr>
<td>21. Game application development</td>
<td>Major lab</td>
</tr>
<tr>
<td><strong>F. Advanced Topics (pipelining/hazards, C-to-assembly)</strong></td>
<td></td>
</tr>
<tr>
<td>22. Pipelined RV32I RISC-V processor architecture, handling hazards</td>
<td>60</td>
</tr>
<tr>
<td>23. C program compilation to RISC-V assembly</td>
<td>30</td>
</tr>
</tbody>
</table>

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**Course homepage**

*Browse course* (top left of browser)

*Use* (top right of browser)
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• Future work (inviting Community participation/collaboration)
• Use remote (FPGA) hardware [3]
• ARM Processing System (controller) and Programmable Logic (PL) (entity)
• Architecture supports [3]
  • Centralised vicilologic FPGA resources
  • Distributed FPGA resources
  • Locally-connected FPGAs
Online Course Builder Steps

- User Design (UD) RTL development
  - HDL capture, simulation, logic synthesis
  - Generate FPGA config bitstream and UD metadata

- Upload UD project to server
- Create User Design view
- Create UD lesson step
- Include step in course
- Execute course step

Connect internal signals to probe register

UD User Design

Online course builder (admin)

Client browser

ARM

AXI

Control register

Controller/server

vicilologic

Projects (cfg bitstream, metadata)

Views

Lessons

Courses

Users

Groups

Controller/entity
Online Course Builder Demo

**Demo video:** 4-bit counter

Uses lesson in **VICILOGIC course**

Digital Systems Design and FPGA Prototyping: Fundamentals, HDL and EDA tools

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**User Design (UD) RTL development**

- parse/wrap UD
- Generate FPGA config bitstream and UD metadata

**Online course builder (admin)**

- Upload UD project to server
- Create User Design view
- Create UD lesson step
- Include step in course
- Execute course step

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Course builder commands

- set_text
- set_left_text
- set_view
- write
- loop n  end_loop
- start_batch send_batch
- flash_icons stop_flash_icons
- wait_for_sigs knowledge_check
- allow_view_clicks stop_view_clicks
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Memory Store/Load Instructions Demo

- **Memory store/load**
- Demonstrates
  - Store/load data transfer
  - Signal widget highlighting
5-Stage Pipeline reg-imm Instruction Demo

• 5-stage RV32I pipeline execution instruction \texttt{addi x1, x0, 0x35}

• **Demonstrates**
  • Pipelined register operation
  • Interactive timing diagram
  • Instruction stage execution in pipeline table
Game Application Demos

• Game applications
• Assembly language
• Peripherals
  • RNG counter
  • In/out ports
• RISC-V debug interface
• Future
  • extend peripherals for development of range of low-end embedded applications
Unit-level Component Lessons

Course Section/Topics

D. RV32I Processor hardware design (HDL capture-to-prototype), memory-mapped peripherals
+ 17. IF PCCU/IM, ID DEC/RB, EX EX/ALU, MEM memory, WB writeback 30
+ 18. RV32I Hardware Description Language model capture, simulation, logic synthesis, prototype (remote FPGA) Major lab
+ 19. Memory-mapped peripheral components applications 45
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User Experience / Feedback

• Course lesson ratings (1-10), 79%–84%, # respondents

(a) register-immediate instructions
81% / 19

(b) Assembly simulation, remote hardware execution / debug
81% / 13

(c) Register-register instructions
84% / 37

(d) Shift instructions
79% / 20

(e) Branch and loop delay program
79% / 15

(f) LUI Load upper immediate instruction
81% / 19

(g) Memory store-load instructions
80% / 11

Sep-Dec 2020
User Comments

What element(s) of the lessons did you find most useful?

• “labs and exercises”
• “interactive diagrams / coloured widgets”
• “visualising internal signals and registers”
• “combination of view and lesson text”
• “video demos”
  • “good flow between reading text and understanding what was happening on hardware”
  • “instruction generator/viewer is really useful”
  • “star widgets highlighting active datapath (indicating where to look)”
  • “signals being shown at the top of the screen (to aid bit-level activity)”
  • “good pace. Being able to prove that I know this stuff”
• “breakdown of instruction step-by-step / thorough coverage”
• “sandboxes”
• “knowledge checks and challenges”
• “example assembly program descriptions and demos”
• “worked examples”
FPGA Usage Stats

• No. of remote FPGA sessions (45 users)
  • 3 week period (Fri 23 Oct–Thu 12th Nov 2020)
  • Each column colour segment highlights the level of configuration/use of a specific FPGA
  • b), c) contribution of individual users
  • a) combined contribution of all users

• 112,000 FPGA configurations since Feb 2018
Future Work

- Collaborate
- Create new courses
- Extend RISC-V peripherals, enabling low-end remote embedded applications
- Continue lesson and browser UI enhancements
- Support Intel FPGAs, Verilog
- Include C-to-assembly compilation tools tutorial
Invitation to Collaborate

• Access courses vicilogic.com/register/
• Available courses vicilogic.com/vicilearn/course/
  • RISC-V® Online Tutor
  • Digital Systems Design and FPGA Prototyping: Fundamentals, HDL and EDA tools
• Share links with students/colleagues
• Collaborate in assembling distributed, shared remote hardware resources (100s of remote FPGAs)
• Collaborate in creating new interactive, online courses, e.g,
  • Cache memory design
  • Hardware pixel processing algorithms
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Thankyou
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