REV International Conference on Remote Engineering and Virtual Instrumentation

VICILOGIC

ENTERPRISE IRELAND where innovation means business

NUI Galway

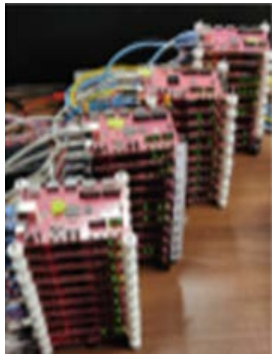
Presentation Video

https://tinyurl.com/RISCVOnlineTutorLinks

RISC-V® Online Tutor

Proceedings of the International Conference on Remote Engineering and Virtual Instrumentation (REV2021)
Hong Kong (Virtual Conference), Feb21, pp 316-328

Fearghal Morgan[1], Arthur Beretta[2], Ian Gallivan[1], Joseph Clancy[1], Frédéric Rousseau[2], Roshan George[1], László Bakó[3], Frank Callaly[1]



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[3]SAPIENTIA - Hungarian University of Transylvania, Targu-Mures/Corunca
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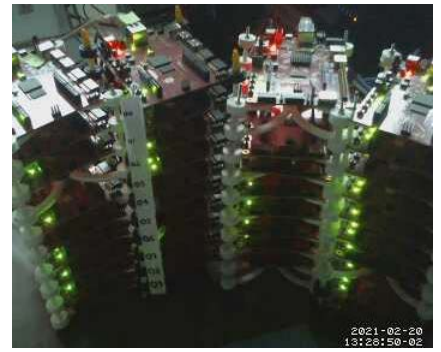
Awarded Runner-up REV2021 Best Full Paper Award



Access course: register at https://www.vicilogic.com/register/

Using VICILOGIC online learning, remote FPGA prototyping and course builder platform

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Presentation Overview

- **RISC-V introduction**
- RISC-V Online Tutor course strategy and demo
- vicilogic Online learning, remote FPGA prototyping, course builder
- RISC-V Online Tutor lesson structure and application program demos
- RISC-V Online Tutor user experience and feedback, FPGA usage stats
- Future work (inviting Community participation/collaboration)

About RISC-V®

RISC-V® Online Tutor

- Free, open Instruction Set Architecture (ISA) (Berkeley 2010)
- Growing community (RISC-V International, industry, university)
- Enabling new era of processor innovation
  - through open standard collaboration
  - Freedom in developing extensible software and hardware
- Custom ICs based on RISC-V will enable cost-effective IoT product differentiation
  - Building custom chips becoming practical, due to evolution of electronic design tools, and lower market entry to semiconductor manufacturing industry
  - Sustainable choice for building custom chips, thanks to adoption/promotion by major technology companies, industrial organisations, governments

(*Gartner Report, June 20*)

RISC-V Training: Call For Participation

RISC-V International riscv.org

- Bare Metal & Real-time OS on RISC-V
- Compliance & Verification
- Debug & Trace
- Formal Specification
- Physical Memory Protection
- The RISC-V Memory Model
- RISC-V Toolchain & Kernel Development

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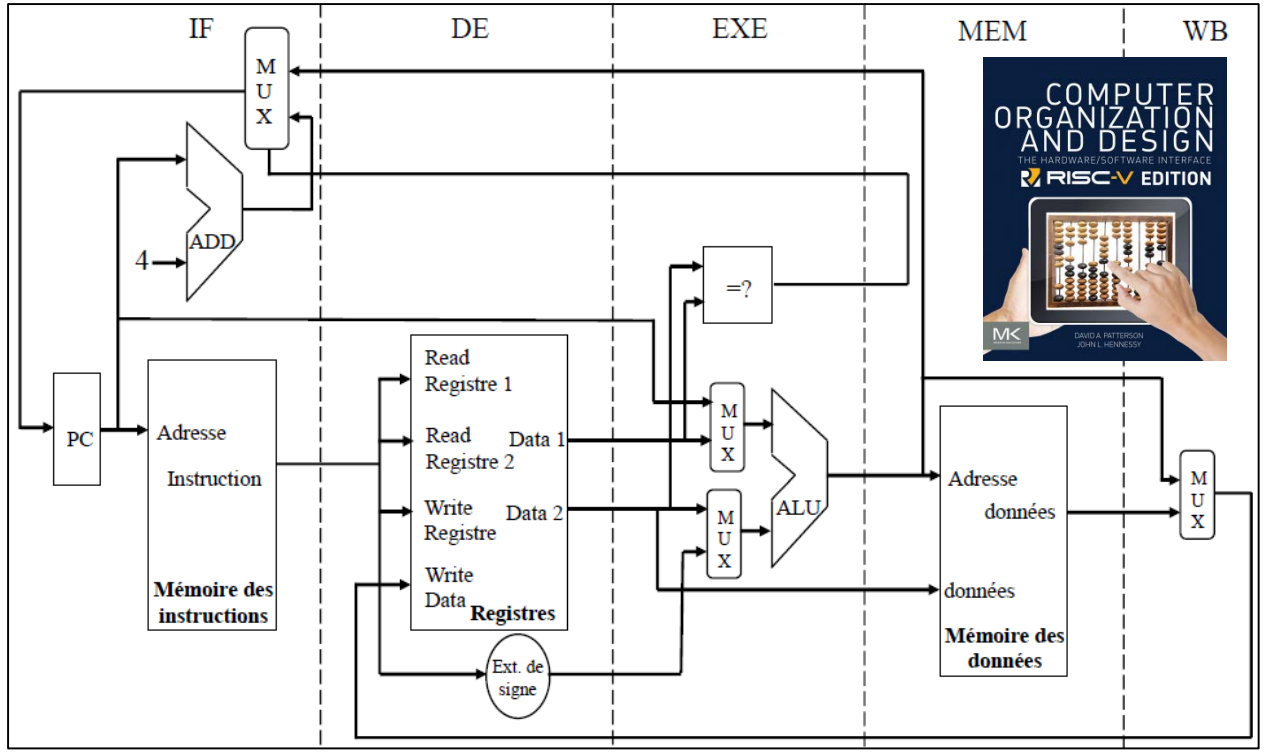
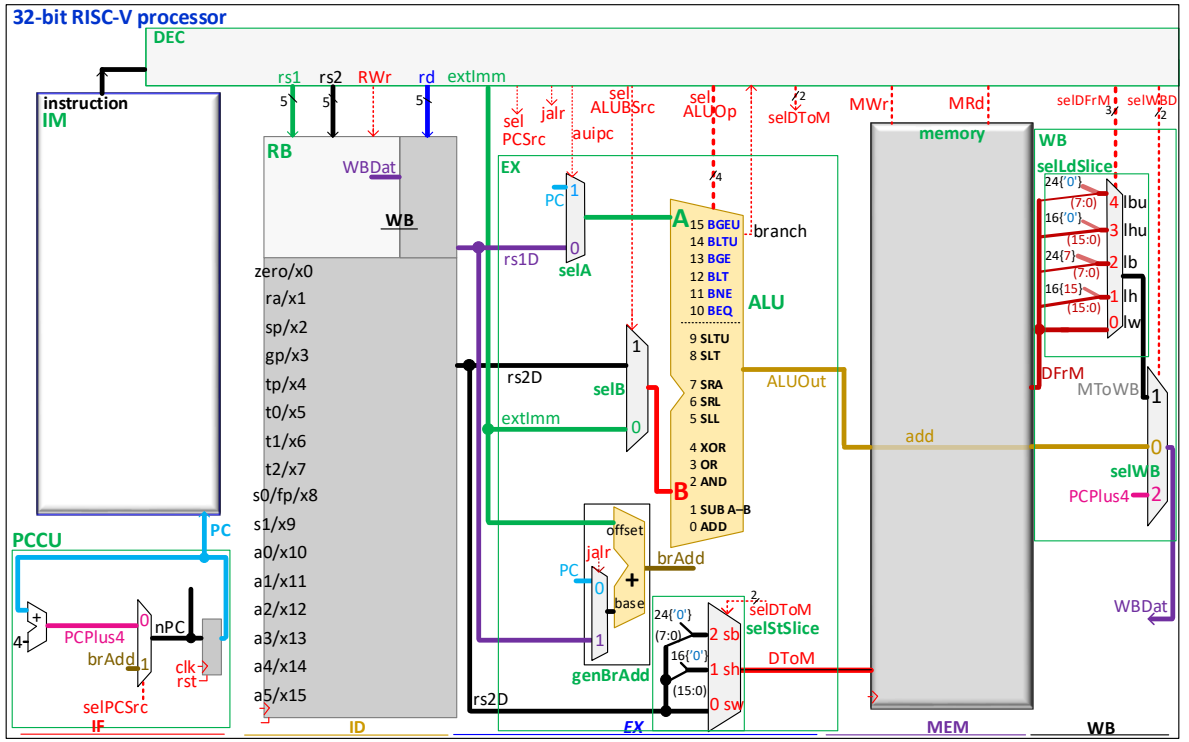
Visualising RV32I RISC-V Architecture

Single cycle datapath diagram



[11] John Hennessy/David Patterson

RISC-V Online Tutor datapath diagram



IF instruction fetch

ID instruction decode

EX execute, address calculation

MEM memory access

WB writeback

RISC-V® Online Tutor: Audience/Strategy

- Target audience
  - Professors/Students, Embedded Systems/IP Developers, Programmers ... interested in RISC-V Fundamentals; what's Inside a RV32I RISC-V processor?
- Integrated training and practice (15 hours online, excluding labs)
- From RISC-V digital logic hardware to C programming
- Lesson strategies
  - Online, self-paced
  - Integrated with remote RISC-V hardware
  - Interactive, learn-by-doing experience, visually-rich
  - Guided-learning, sandboxes, knowledge checks

Course Structure

RISC-V® Online Tutor

From RISC-V digital logic hardware to C programming

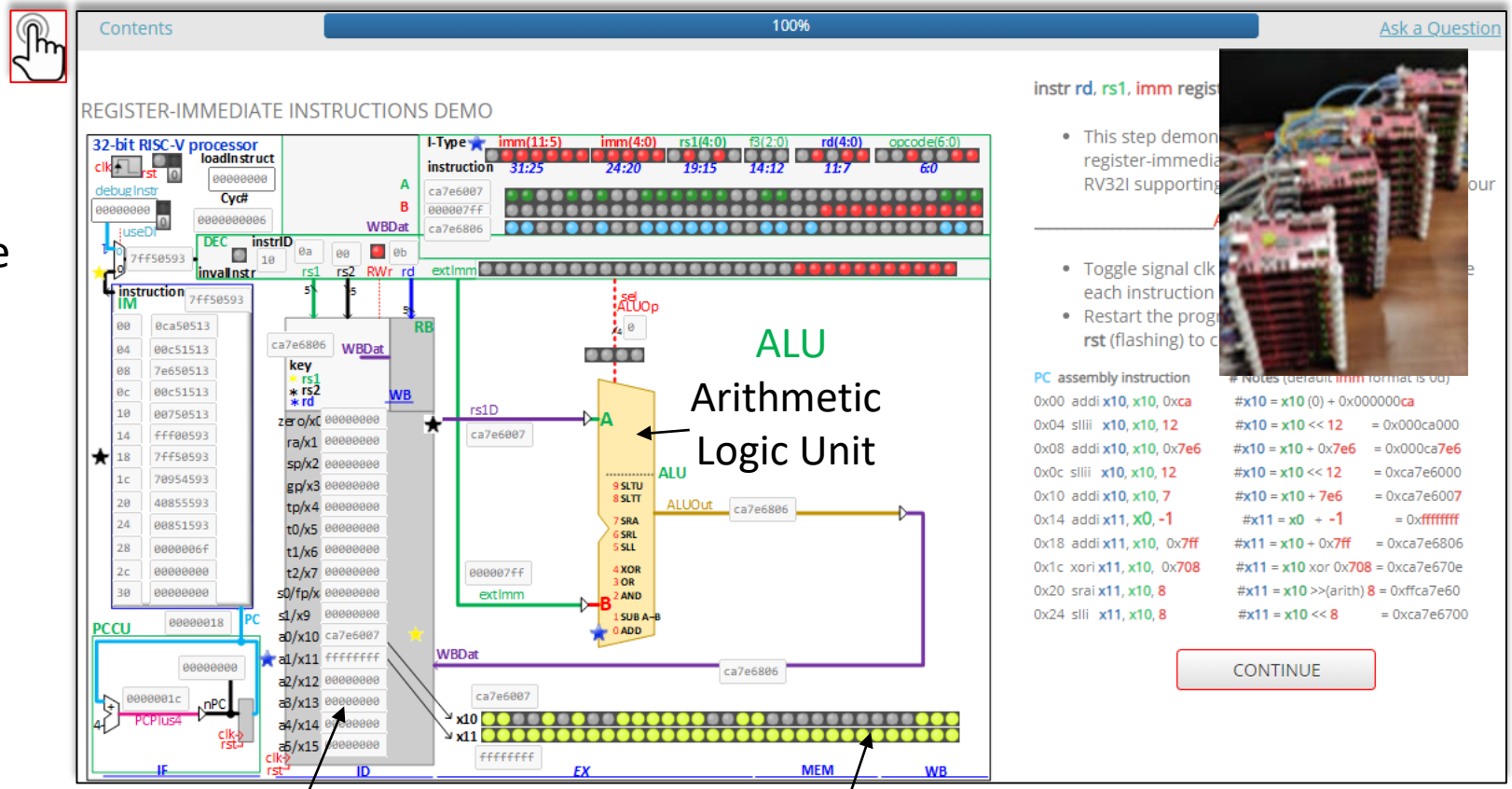
Course homepage

A. Front: introduction, resources, references
B. Tools tutorials
   - Assembly language Venus [7] online simulator
   - Remote RISC-V hardware: program instruction upload, execute, hardware debug
C. RV32I assembly instruction-by-instruction -- processor hardware support
D. RV32I RISC-V hardware design-to-prototype (HDL-based), with memory-mapped peripherals, using industry-standard tools / hardware description language (HDL)
E. Assembly program applications (including games)
F. Advanced Topics: pipelining/hazards, C-to-assembly

Lesson/Framework Demo

RISC-V® Online Tutor

- Register-immediate instruction
- Guided lesson
- Browser (**view** on left side) links to remote RISC-V hardware
- Overlays signal widgets on **view**
- * * * highlight active datapaths
- Remote FPGA tower
- Transparent FPGA allocation, FPGA configuration, browser-FPGA interaction



RB Register Bank x0-x15 x10/x11 LED display

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Detailed Course Structure

RISC-V® Online Tutor

Section/Topics	Duration (min)
A. Intro, resources, references, application demos	
+ 1. Introduction: RISC-V Processor Architecture & Applications	90
2. Learning Outcomes RV32I RISC-V instruction generator and viewer	
2. RV32I RISC-V instruction generator and viewer	
3. RISC-V references	
4. Tour of vicilogic online learning and prototyping platform	
+ 5. Game application demos (executing on remote RISC-V)	
B. Program execution tools tutorials (simulation/remote hardware)	
+ 5. Assembly programming, simulate, hardware execution and debug	120
C. RV32I assembly instructions and processor architecture support	
+ 6. **addi** register-immediate	120
+ 7. **add/sub** register-register	40
+ 8. Register-immediate **addi**, **xori**, **ori**, **andi**, **slti**, **sltiu**	60
+ 9. Register-register **add**, **sub**, **xor**, **or**, **and**, **slt**, **sltu**	20
+ 10. Constant-shift **slli**, **srli**, **srai**, register-shift **sll**, **srl**, **sra**	35
+ 11. **lui** load upper immediate	15
+ 12.**beq**, **bne**, **blt**, **bge**, **bltu**, **bgeu** branch Program: delay loop	50
+ 13.Program: shift x10 register left each sec **lui, add, addi, slli, bne**	25
+ 14. Store/load to/from memory **sw**, **sh**, **sb**, **lw**, **lh**, **lb**, **lhu**, **lbu**	60
+ 15. **auipc** add upper immediate to PC	20
+ 16. **jal/jalr** jump and link	25

Section/Topics	Duration (min)
D. RV32I Processor hardware design (HDL capture-to-prototype), memory-mapped peripherals	
+ 17. **IF** PCCU/IM, **ID** DEC/RB, **EX** EX/ALU, **MEM** memory, **WB** writeback	30
+ 18. RV32I Hardware Description Language model capture, simulation, logic synthesis, prototype (remote FPGA)	Major lab
+ 19. Memory-mapped peripheral components applications	45
E. Assembly program applications (game app development)	
+ 20. Functions and stack handling	40
+ 21. Game application development	Major lab
F. Advanced Topics (pipelining/hazards, C-to-assembly)	
+ 22. Pipelined RV32I RISC-V processor architecture, handling hazards	60
+ 23. C program compilation to RISC-V assembly	30

Course homepage

Browse course Contents (top left of browser)

Use Ask a Question (top right of browser)

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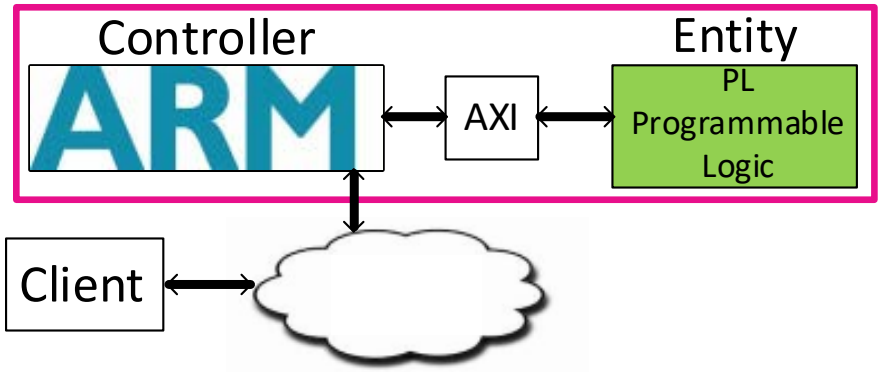
VICILOGIC Online Learning/Prototyping/Course Builder

- Use remote (FPGA) hardware [3]
- ARM Processing System (controller) and Programmable Logic (PL) (entity)



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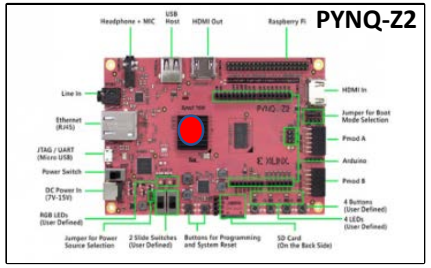
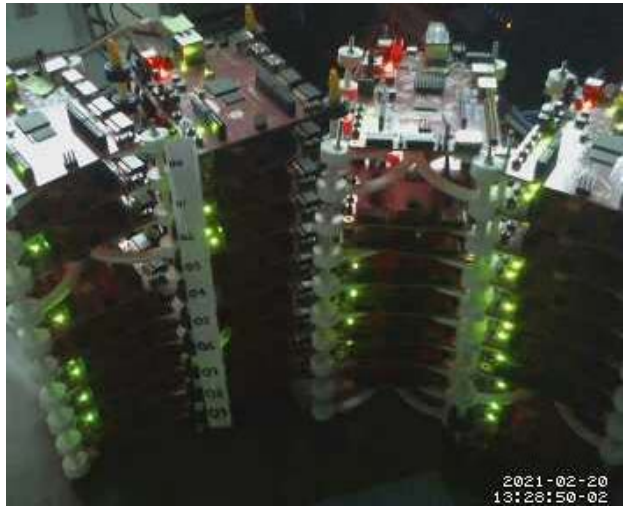
VIVADO



intel FPGA
Quartus Prime
Design Suite

DE10-Nano



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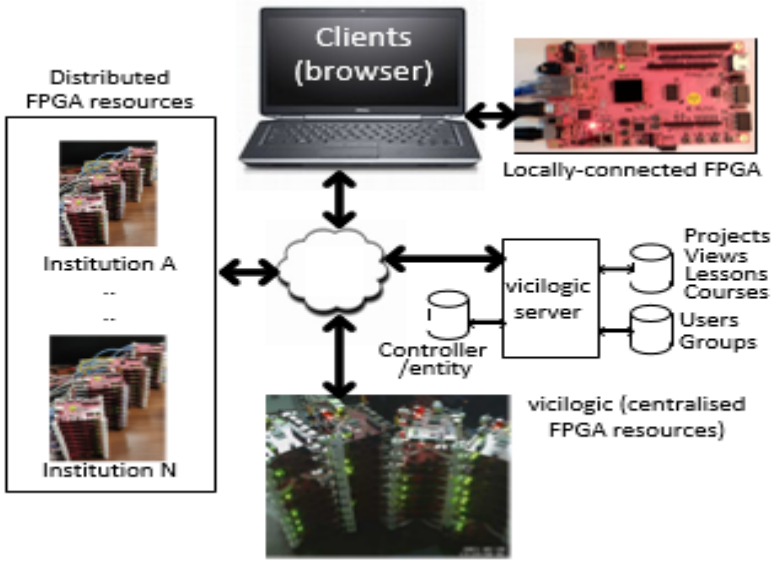
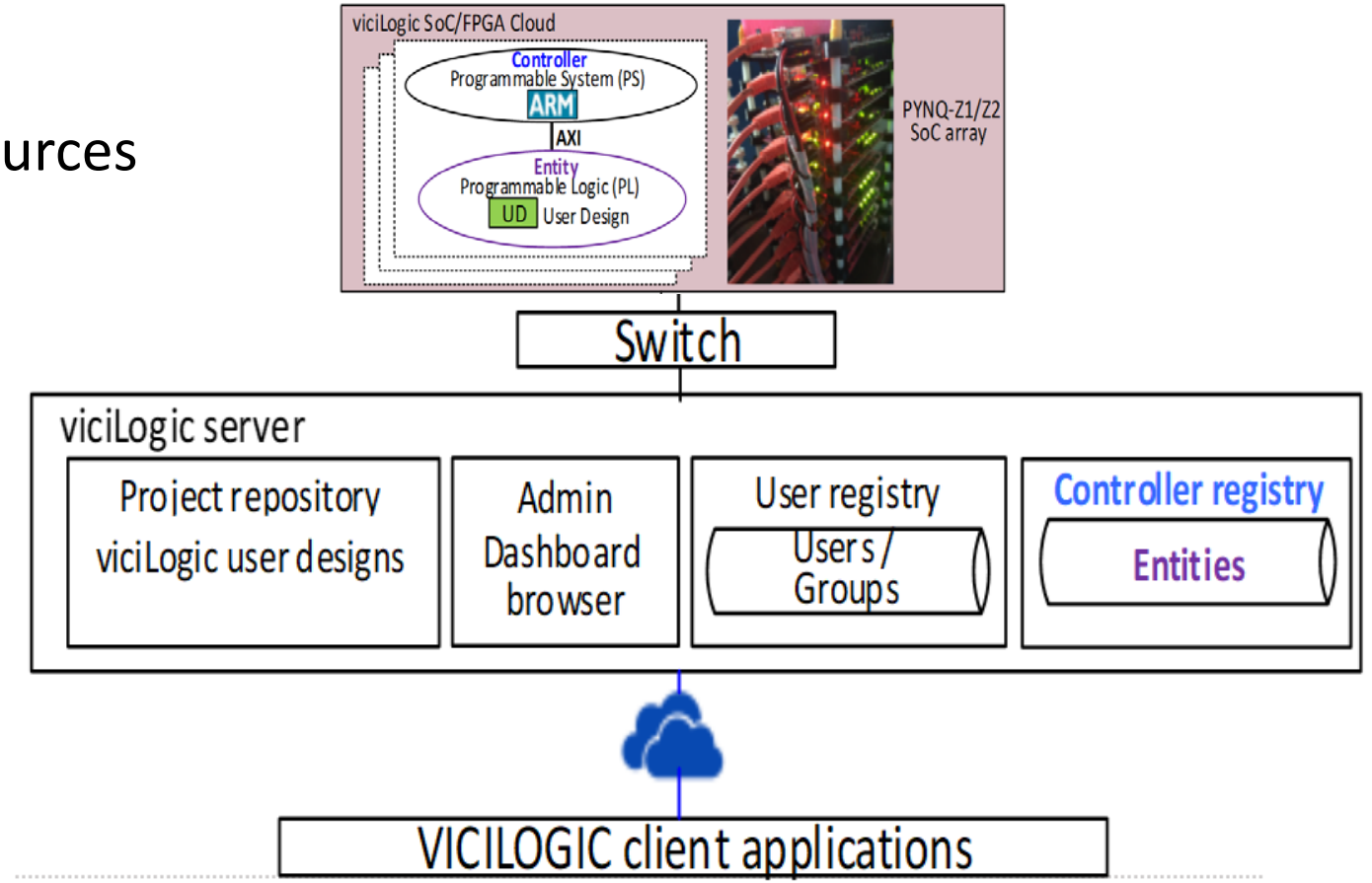
VICILOGIC Online Learning/Prototyping/Course Builder

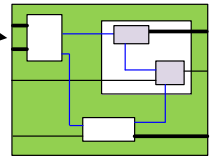
- Architecture supports [3]
  - Centralised vicilogic FPGA resources
  - Distributed FPGA resources
  - Locally-connected FPGAs





VICILOGIC Online Course Builder Steps

User Design (UD) RTL development



UD User Design
HDL capture, simulation, logic synthesis

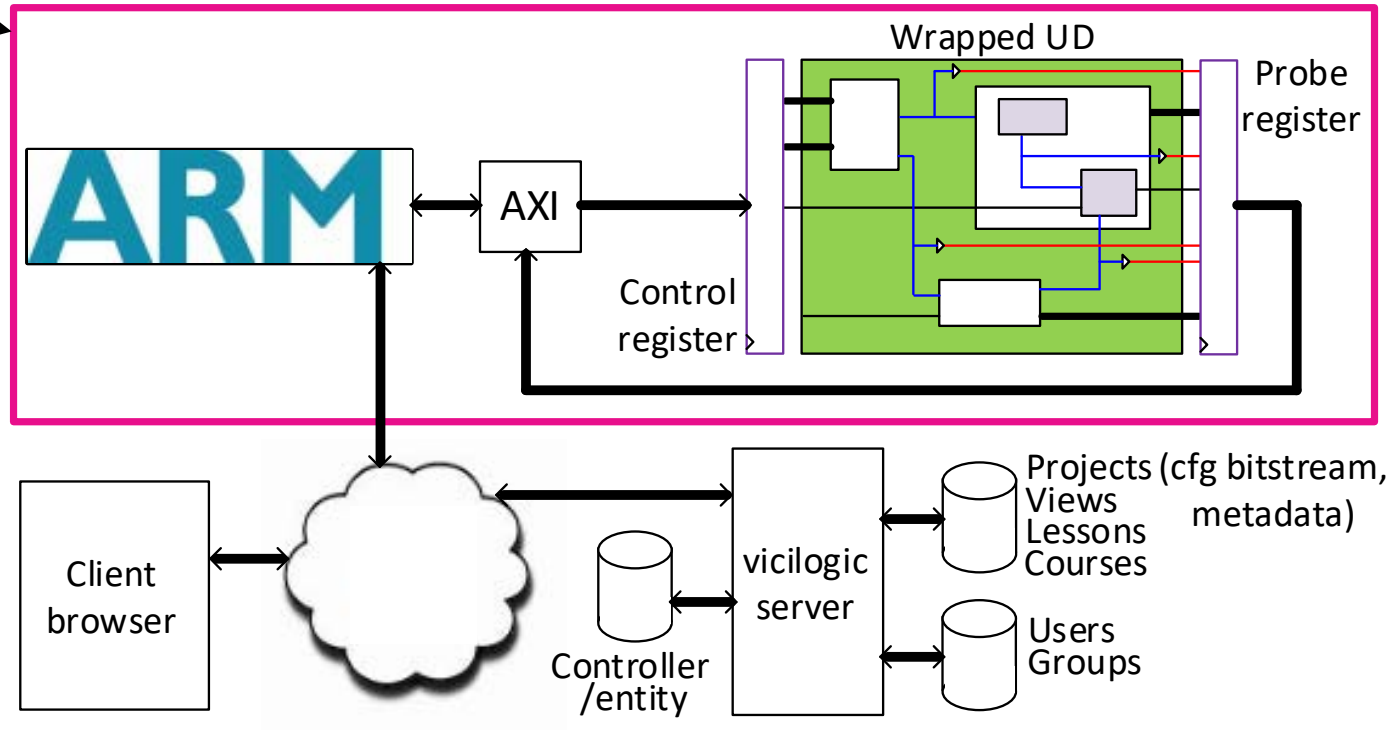
VICILOGIC parse/wrap UD

VIVADO Generate FPGA config bitstream and UD metadata

VICILOGIC Online course builder (admin)

- Upload UD project to server
- Create User Design view
- Create UD lesson step
- Include step in course
- Execute course step

Connect internal signals to probe register



VICILOGIC Online Course Builder Demo

User Design (UD) RTL development

VICILOGIC parse/wrap UD

VIVADO Generate FPGA config bitstream and UD metadata

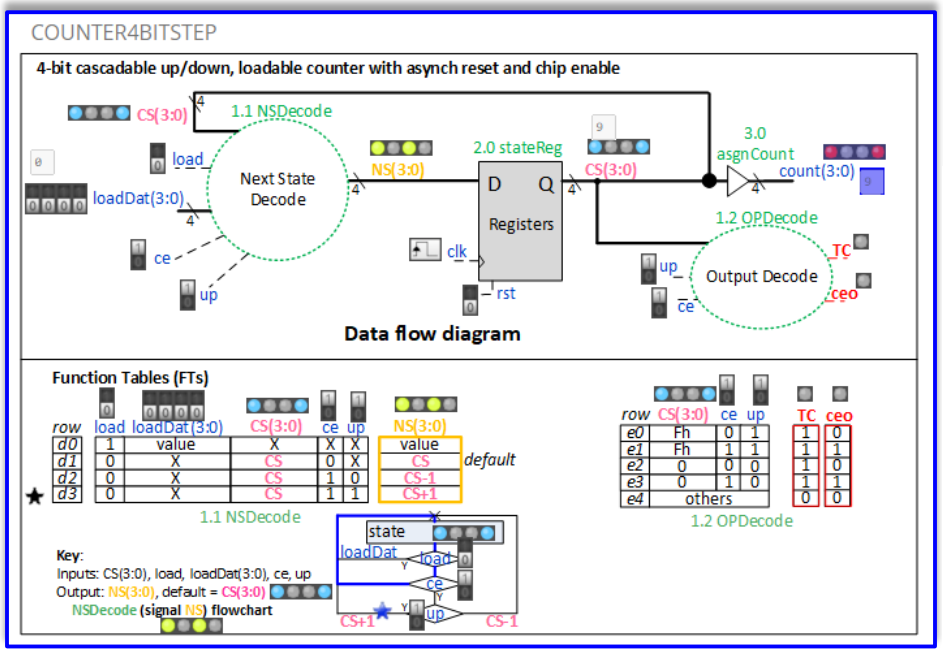
VICILOGIC Online course builder (admin)

- Upload UD project to server
- Create User Design view
- Create UD lesson step
- Include step in course
- Execute course step

Demo video: 4-bit counter

Uses lesson in VICILOGIC course

Digital Systems Design and FPGA Prototyping: Fundamentals, HDL and EDA tools



Course builder commands

```
set_text
set_left_text
set_view
write
loop n    end_loop
start_batch   send_batch

flash_icons     stop_flash_icons
wait_for_sigs
knowledge check
allow _view_clicks
stop_view_clicks
```

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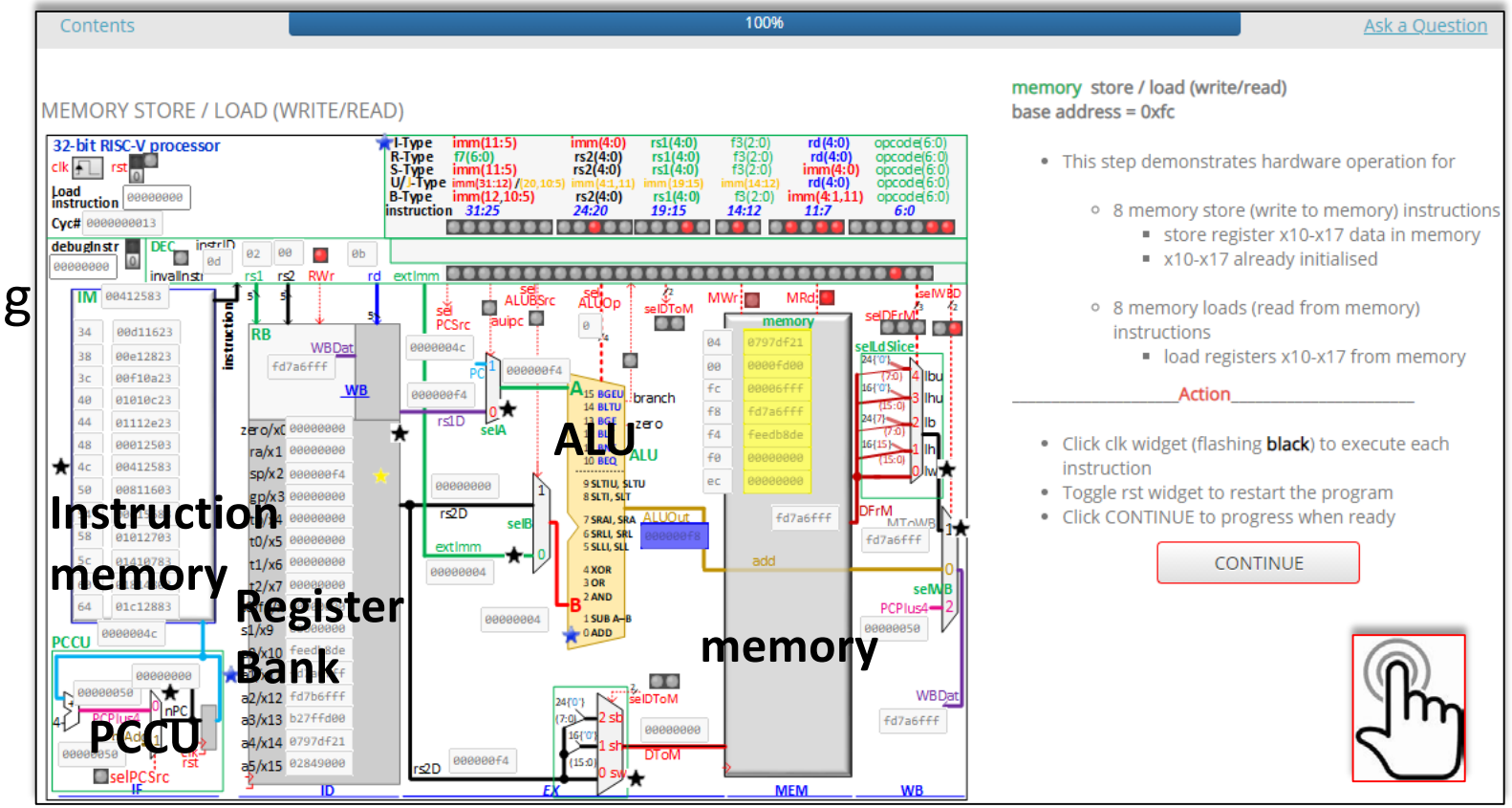
Memory Store/Load Instructions Demo

- Memory store/load
- Demonstrates
  - Store/load data transfer
  - Signal widget highlighting

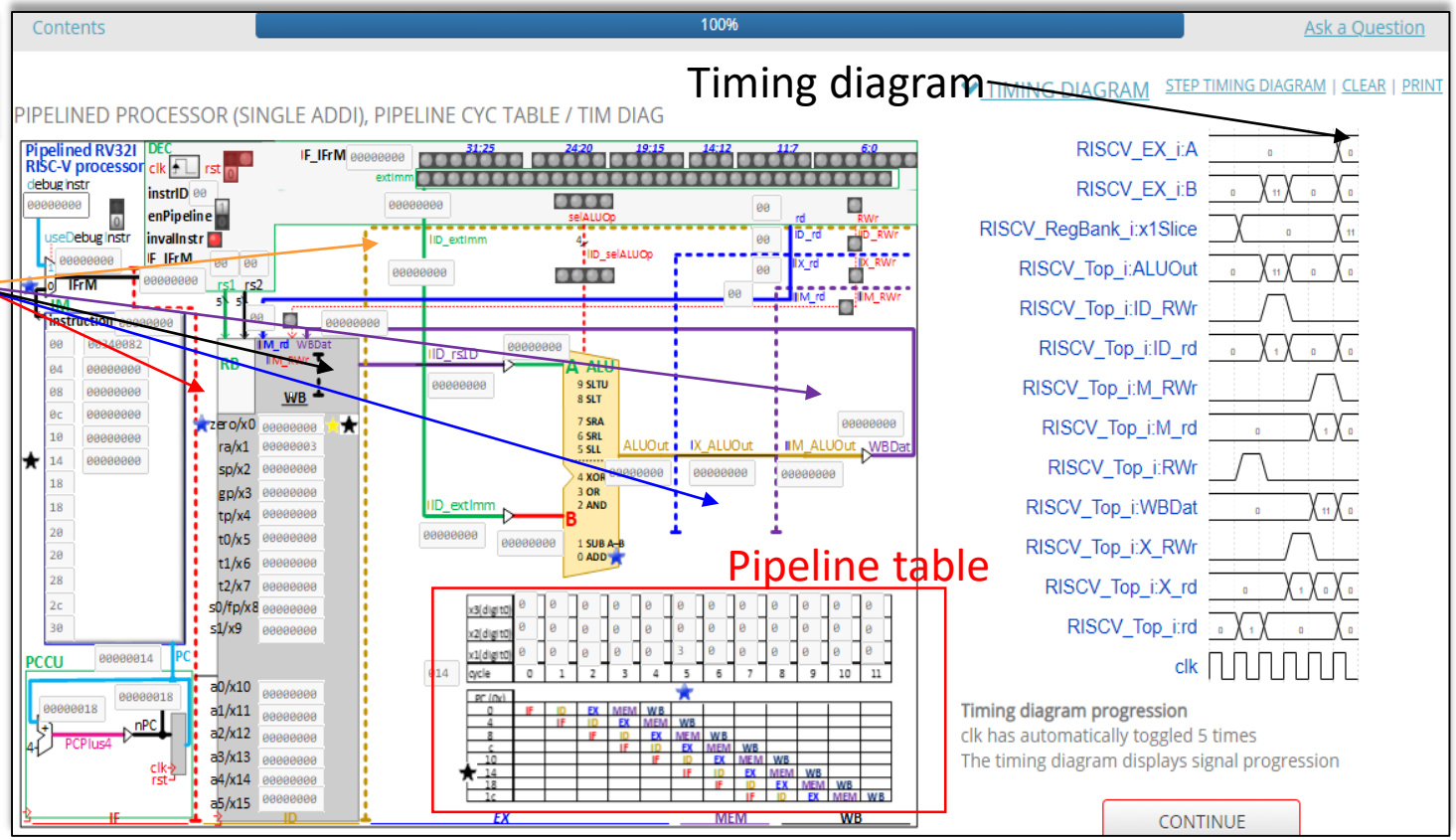


5-Stage Pipeline reg-imm Instruction Demo

- 5-stage RV32I pipeline execution
  instruction **addi x1, x0, 0x35**

Pipeline registers

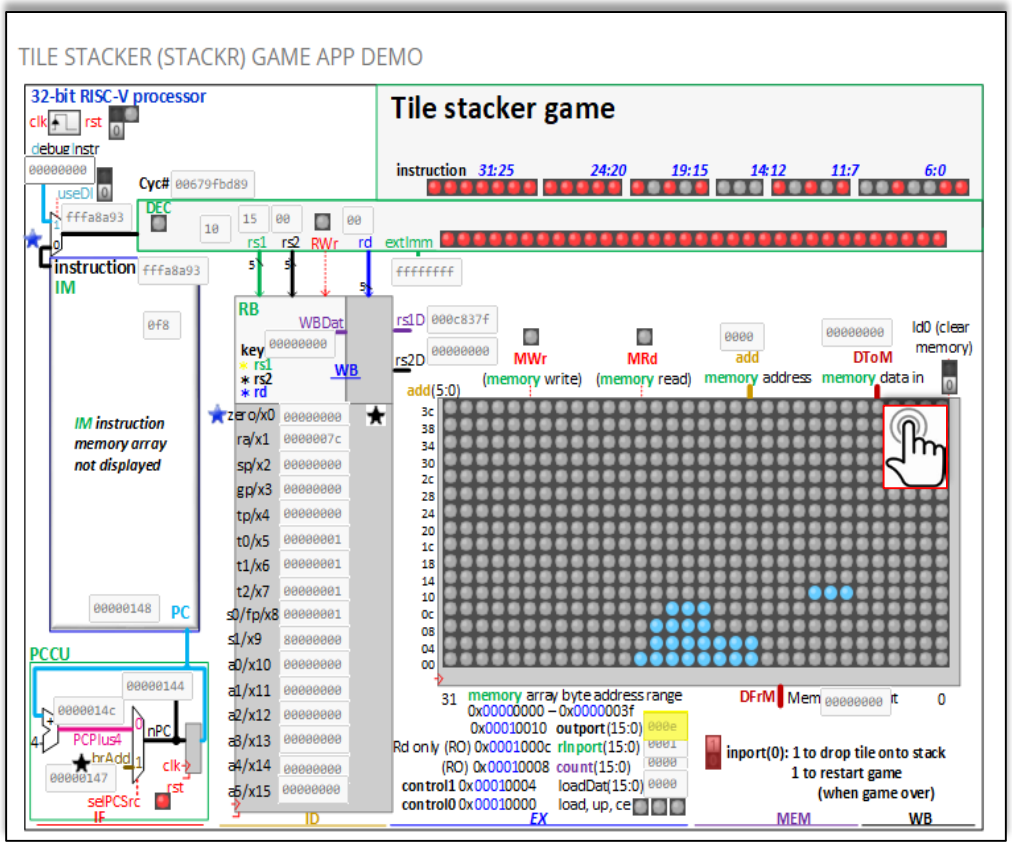
- Demonstrates
  - Pipelined register operation
  - Interactive timing diagram
  - Instruction stage execution in pipeline table

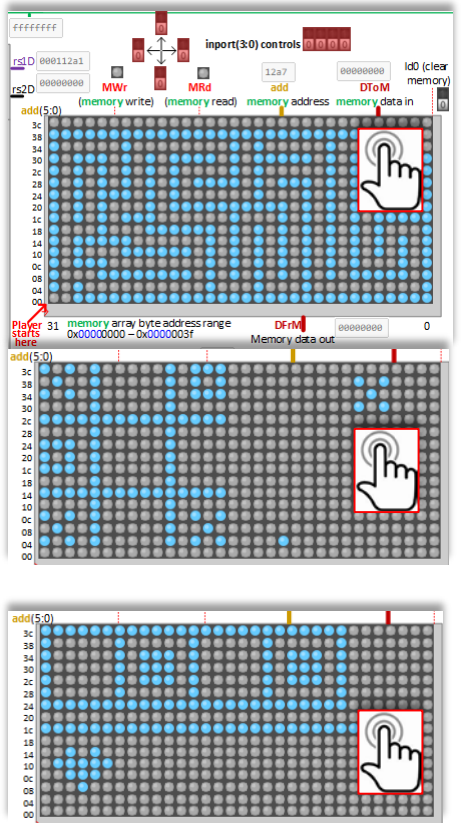


Game Application Demos

RISC-V® Online Tutor

- Game applications
- Assembly language
- Peripherals
  - RNG counter
  - In/out ports
- RISC-V debug interface
- Future
  - extend peripherals for development of range of low-end embedded applications





Unit-level Component Lessons

RISC-V® Online Tutor [2]

Course Section/Topics	Duration (min)
D. RV32I Processor hardware design (HDL capture-to-prototype), memory-mapped peripherals	
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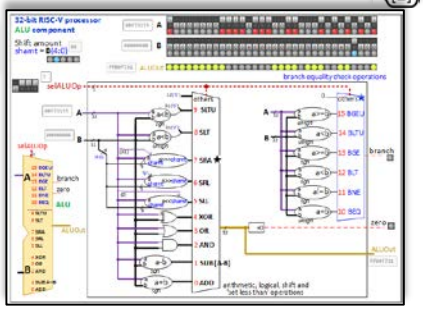
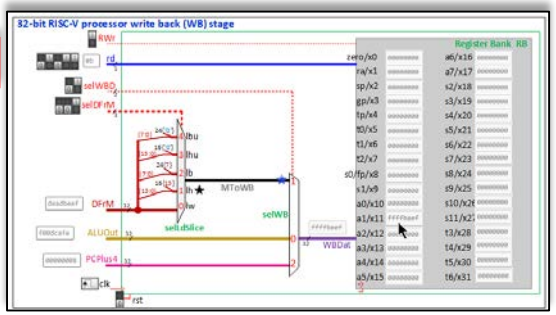
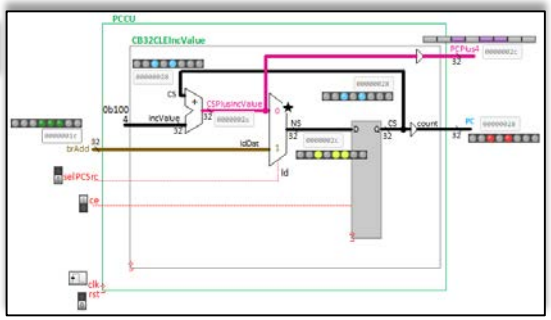
ALU



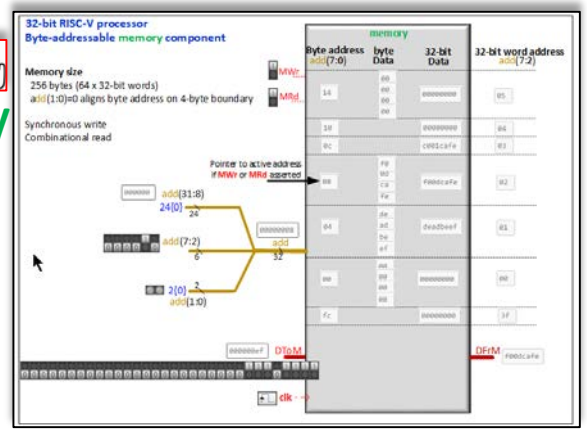
WB



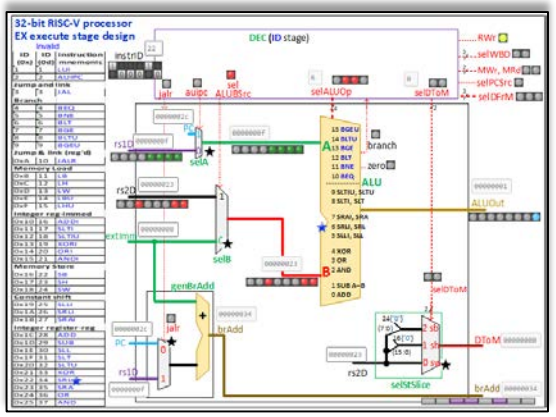
PCCU



memory



EX



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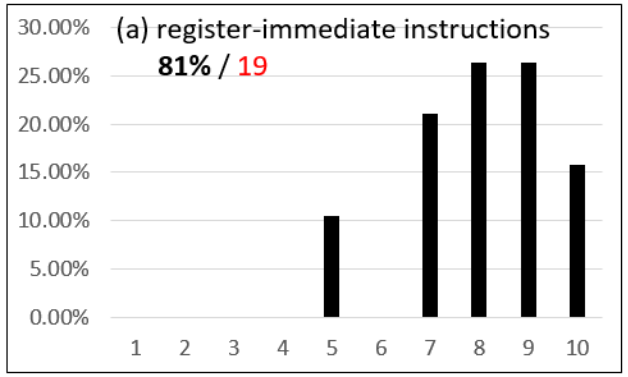
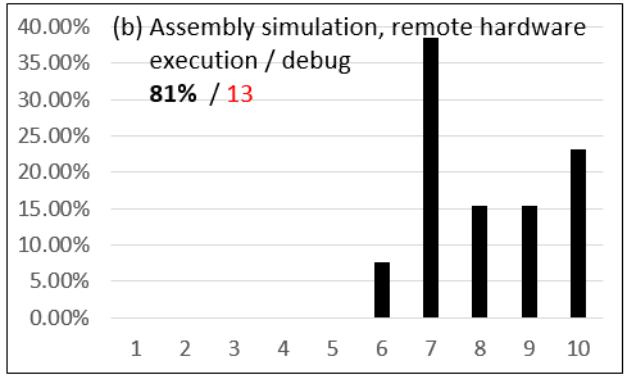
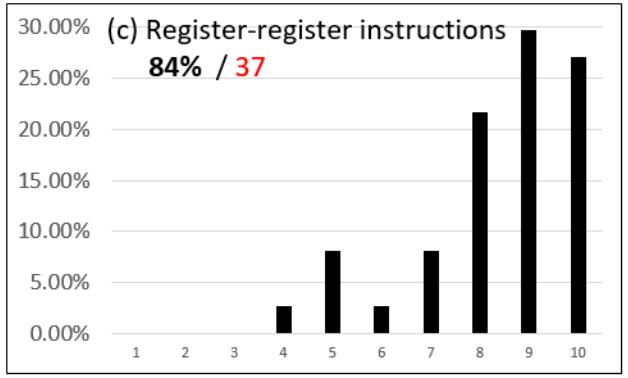
User Experience / Feedback

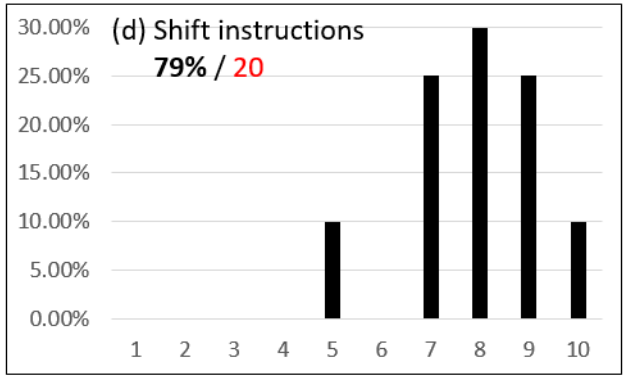
RISC-V® Online Tutor [2]

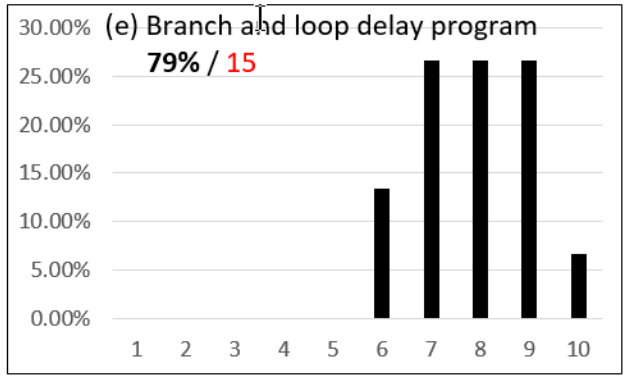
- Course lesson ratings (1-10), 79%–84%, # respondents

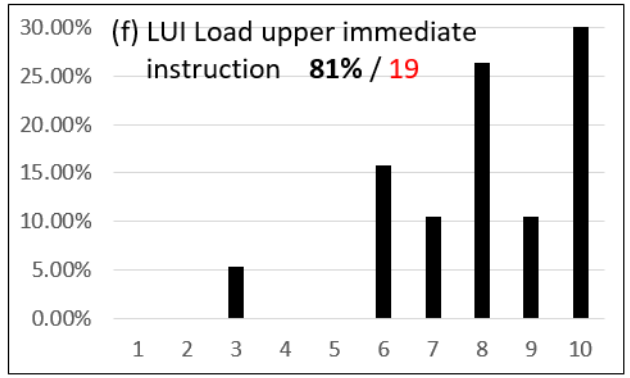




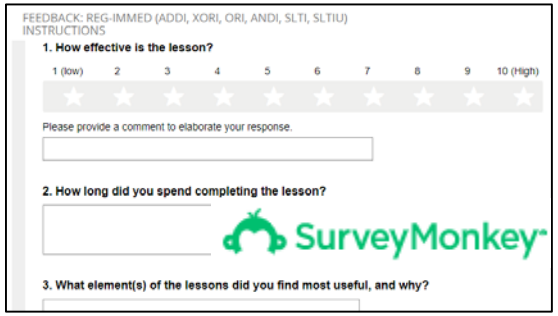


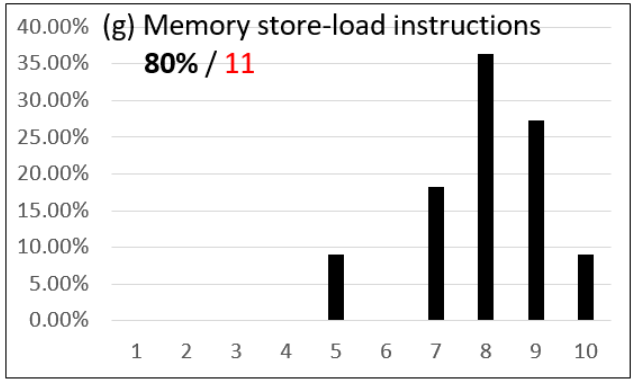






End of lesson surveys





Sep-Dec 2020

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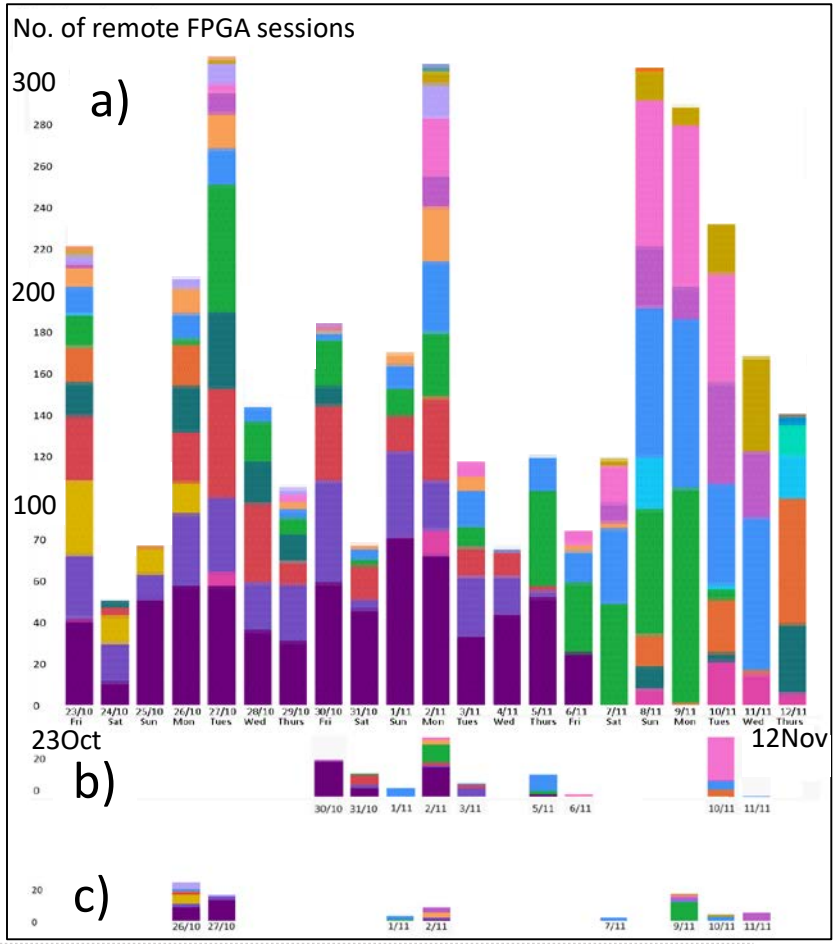
User Comments

What element(s) of the lessons did you find most useful?

- ”labs and exercises”
- ”interactive diagrams / coloured widgets”
- ”visualising internal signals and registers”
- ”combination of view and lesson text”
- ”video demos”
- ”breakdown of instruction step-by-step / thorough coverage”
- ”sandboxes”
- ”knowledge checks and challenges”
- ”example assembly program descriptions and demos”
- ”worked examples”
- ”good flow between reading text and understanding what was happening on hardware”
- ”instruction generator/viewer is really useful”
- ”star widgets highlighting active datapath (indicating where to look)”
- ”signals being shown at the top of the screen (to aid bit-level activity)”
- ”good pace. Being able to prove that I know this stuff”

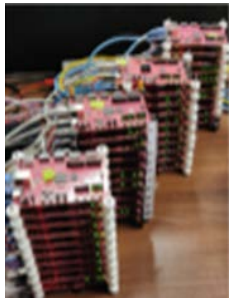
FPGA Usage Stats

- No. of remote FPGA sessions (45 users)
  - 3 week period (Fri 23 Oct–Thu 12th Nov 2020)
  - Each column colour segment highlights the level of configuration/use of a specific FPGA
  - b), c) contribution of individual users
  - a) combined contribution of all users
- 112,000 FPGA configurations since Feb 2018

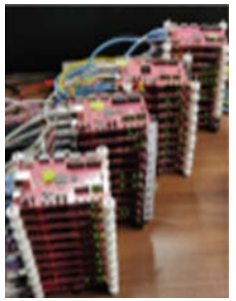


Future Work

- Collaborate
- Create new courses
- Extend RISC-V peripherals, enabling low-end remote embedded applications
- Continue lesson and browser UI enhancements
- Support Intel FPGAs, Verilog
- Include C-to-assembly compilation tools tutorial

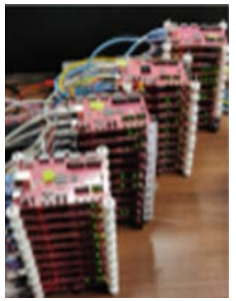


Invitation to Collaborate



- Access courses vicilogic.com/register/
- Available courses vicilogic.com/vicilearn/course/
  - RISC-V® Online Tutor
  - Digital Systems Design and FPGA Prototyping: Fundamentals, HDL and EDA tools
- Share links with students/colleagues
- Collaborate in assembling distributed, shared remote hardware resources (100s of remote FPGAs)
- Collaborate in creating new interactive, online courses, e.g,
  - Cache memory design
  - Hardware pixel processing algorithms

Invitation to Collaborate



- Access courses vicilogic.com/register/
- Available courses vicilogic.com/vicilearn/course/
  - RISC-V® Online Tutor
  - Digital Systems Design and FPGA Prototyping: Fundamentals, HDL and EDA tools
- Share links with students/colleagues
- Collaborate in assembling distributed, shared remote hardware resources (100s of remote FPGAs)
- Collaborate in creating new interactive, online courses, e.g,
  - Cache memory design
  - Hardware pixel processing algorithms

Thankyou

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